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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,990	03/08/2001	Yasuo Tarui	F-6888	5855

7590

04/13/2004

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EXAMINER

TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/801,990

Applicant(s)

TARUI ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 March 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 March 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/22/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to for the following reasons.

Figures 12, 13, 14, 15 and 16 are not designated by a legend such as "Prior Art".

The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Applicant is required to submit a proposed drawing correction, showing changes in red ink, in response to this Office action. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner (see MPEP § 608.02v).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,140,672 to Arita et al.

Regarding to claim 1, Arita et al. discloses a transistor-type ferroelectric nonvolatile memory element having an MFMISS (metal-ferroelectric-metal-insulator-semiconductor) structure, comprising an MFM 14 (metal-ferroelectric-metal) structure and an MIS 13 (metal-insulator-semiconductor) structure stacked up and down; and means for increasing the effective area of a capacitance of the lower MIS structure as compared with the effective area of a capacitance of the upper MFM structure as set forth in col. 5, lines 49-67, lines 1-3, col. 7, lines 1-50, and fig. 1.

Regarding to claim 2, a transistor-type ferroelectric nonvolatile memory element further having a semiconductor substrate 32 and a trench 38 formed in the semiconductor substrate 32, wherein the MIS structure 13 is formed in the trench 38, the MFM structure 14 is laminated on the trench 38 nearly in parallel with the main surface of the semiconductor substrate 32, and means for increasing the effective area in the trench (col. 6, lines 63-67, col. 7, lines 1-61, and fig. 1).

Regarding to claim 5, a transistor-type ferroelectric nonvolatile memory element, wherein the MIS structure is a MIS transistor of the nonvolatile memory element, and the regions of source and drain of the MIS transistor are isolated by the trench (col. 7, lines 1-36, and fig. 1).

Regarding to claim 6, a transistor-type ferroelectric nonvolatile memory element, wherein the MIS structure includes a rugged portion therein, means for increasing the effective area is constituted by the rugged portion, the upper part of the MIS structure is flat, and the MFM structure is laminated thereon (fig. 1).

Regarding to claim 7, a transistor-type ferroelectric nonvolatile memory element, wherein means for increasing the effective area is constituted by an MIM (metal-insulator-metal) structure provided between the MFM structure and the MIS structure (fig. 1).

Claim 8 is rejected under the same rationale set forth above to claim 2-7.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,140,672 to Arita et al. in view of Matsuki (6,121,083).

Regarding to claims 3 and 4, Arita et al. disclose a transistor-type ferroelectric nonvolatile memory element, wherein the MIS structure 13 is an MIS transistor of the nonvolatile memory element, the regions of source 26, base 22 and drain 28 of the MIS transistor are formed in the semiconductor substrate 32 in order of source, base and drain from the lower side (col. 7, lines 1-24, and fig. 1).

Arita et al. does not disclose means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench. However, Matsuki teaches means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench (col. 5, lines 17-32, and fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form means for increasing the effective area is a gate structure of the MIS transistor formed on the inner surface of the trench, as taught by Matsuki in order to form a semiconductor memory device that operates at a higher rate, has a greater capacity for storing data therein, and operates in less power consumption (col. 1, lines 10-13).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Mai-Huong Tran



David Nelms
Supervisory Patent Examiner
Technology Center 2800